

DPS2025 Timetable (tentative)

November 13 (Thu)		November 14 (Fri)		
8:10	Registration	8:10	Registration	
8:20				
8:30				
8:40				
8:50				
9:00				
9:10	Opening Remark / Award Ceremony	9:10	Session F AS2. Atomic layer processes (ALE/ALD/ASD) for ultimate control of surface reaction	
9:20				
9:30				
9:40				
9:50				
10:00				
Nishizawa Award Lecture Masaru Izawa (Hitachi High-Tech Corporation) "Understanding Plasma Etching Processes through Surface Reaction Models"		F-1 <Invited> Christophe Vallee (University at Albany) "Engineering plasma for atomic scale processing: ALD, ALE and ASD"		
10:10	Break 10min	10:10	F-2 H. Liu (Tokyo Electron Technology Solutions Ltd.) "Selective Surface Passivation to Unlock High Temperature Area Selective ALD SIN"	
10:20	A-1 <Invited> Sung-II Cho (Samsung Electronics Co., Ltd.) "Breaking new ground : From current progress to future innovations in HARC etching technology"	10:20	F-3 N. Tamaoki (Univ. of Tokyo) "Simulation-Based Prediction of Metal-ALD Growth per Cycle using Molecular Dynamics with Neural Network Potentials"	
10:30		10:30	Session G Computational Approaches (Modeling, Simulation, Machine Learning, AI, Informatics, DX) for Dry Process	
10:40		10:40		
10:50		10:50		
11:00		11:00		
11:10		11:10		
11:20	11:20			
11:30	A-2 <Invited> Thorsten Lill (Lam Research Corporation) "Ion scattering during cryo etching of silicon oxides and nitrides"	11:30	G-4 Y. Sunwoo (Ulsan National Institute of Science and Technology) "Atomistic Insights into Plasma-Material Interactions: Ion Bombardment Driven Crystallization and Pressure Dependent Radical Transportation"	
11:40	Poster Session Day1 (80min)	11:40	Poster Session Day2 (80min)	
11:50				
12:00				
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13:00				
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13:20	Lunch Break 13:00-14:20 (80min)	13:20	Lunch Break 13:00-14:20 (80min)	
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15:00	B-1 J. Hoang (Lam Research Corp.) "Deposition and Etch Co-Optimization for Merged 3D NAND Memory Hole and Interlayer Dielectric Contact Etches"	15:00	H-1 <Invited> Jeongsoo Kim (imec) "Dry etch process technology for 3D-IC and advanced packaging"	
15:10	B-2 T.Kurushima (Nagoya Univ.) "Effect of Gas-Phase Radical Composition Ratio on C _{xF_y} Sticking Probability in High-Aspect-Ratio Holes"	15:10	Session H AS3. Dry process technology for 3D-IC and advanced packaging	
15:20	B-3 K. Tanaka (Daikin Industries, Ltd.) "Novel Additive Gas Development for HF-based Cryogenic HAR Dielectric Etching using Digital Twin"	15:20		
15:30	Break 20min	15:30		
15:40	C-1 M. Sekine (Nagoya Univ.) "Role of H ₂ O in SiO ₂ cryogenic etching using HF plasma"	15:40		
15:50	C-2 T. Imamura (Hitachi, Ltd.) "Depth control of protection layer for HF gas etching via TMSDMA vapor exposure"	15:50		
16:00	C-3 M. Sekine (Nagoya Univ.) "Role of H ₂ O in SiO ₂ cryogenic etching using HF plasma"	16:00		
16:10	D-1 D. Kim (Nagoya Univ.) "Quantitative evaluation of the influence of ion-neutral collisions in the sheath on ion angular distributions"	16:10	H-3 E. Dupuy (imec) "High aspect ratio gate etching for monolithic CFET"	
16:20	Session B AS1. Understanding the mechanisms for future high-aspect-ratio etching technology	16:20	I-1 A. Fathzadeh (Ku Leuven / imec) "Transient Assisted Processing (TAP) a novel scalable plasma processing approach for precision etching and sustainability in semiconductor manufacturing"	
16:30		16:30		
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17:00		17:00		
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17:20	Session C Etching Technologies	17:20	I-2 T. Tillocher (GREMI - Univ. of Orleans/CNRS) "Investigation of adsorbed species in cryogenic etching of SiO ₂ by SF ₆ /H ₂ plasma"	
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19:00	Session D Plasma Diagnostics and Monitoring Systems	19:00	19:00	
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20:40	Session E AS2. Atomic layer processes (ALE/ALD/ASD) for ultimate control of surface reaction	20:40	Session I New Dry Process Concepts	
20:50		20:50		
21:00		21:00		
Banquet		21:00		